KEYNOTES

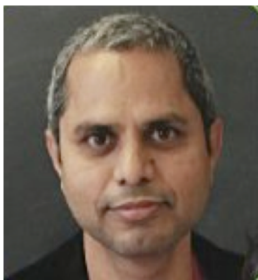
Sylvestre MAURICE (sylvestre.maurice@irap.omp.eu), IRAP (France) - *ChemCam instrument on the Curiosity rover: from R&D to operations on Mars ; be reliable or die…*

The ChemCam project started as an R&D program at Cnes in 2001, was selected by NASA in 2005, launched in 2011, and is operated on the Curiosity rover at Mars since 2012. It consists of a high energy laser which creates, at distance, a plasma on Mars soils and rocks to infer their elemental composition. Quality and reliability were inherent to the development of this very innovative instrument that has to work in a very unusual environment (Mars surface) at 350 million km distance, for the first time on "the most complex robot ever done by JPL", in the end to find out if Mars was in the past an habitable world. I'll trace back this unique experience with emphasis on Quality and Reliability management.

Sylvestre MAURICE is the Deputy Principal Investigator for ChemCam. Along with Principal Investigator Roger Wiens, he is responsible for the design, construction, testing, and delivery of the LIBS instrument. He has previously worked on several projects including Cassini at Saturn, Lunar Prospector orbiting the Moon, and Mars Odyssey that have prepared him for the challenge of building an instrument for Mars exploration.

Ramesh KARRI (rkarri@poly.edu), Université de NY (USA) - *Towards Hardware Cyber security*

Hardware security and trust is an important design objective similar to power, performance, reliability and testability. I will highlight why hardware security and trust are important objectives from the economics, security, and safety perspectives. Important messages from this talk include (i) understanding simple gotchas when traditional DFT, test, and validation techniques are used (scan chains, JTAG, SoC test, assertion based validation), (ii) understand how traditional DFT, test and validation techniques can be used to improve hardware security and trust and finally (iii) understand "Design for Trust" approaches that can provide testability without compromising security and trust.



Ramesh Karri is a Professor of Electrical and Computer Engineering at Polytechnic School of Engineering, New York University. He has a Ph.D. in Computer Science and Engineering, from the University of California at San Diego. His research interests include trustworthy ICs and processors; High assurance nanoscale IC architectures and systems; VLSI Design and Test; Interaction between security and reliability.

He has over 150 journal and conference publications in these areas. These include two tutorial articles in IEEE Computer and three tutorial articles in Proceedings of IEEE on Trustworthy Hardware.

He was the recipient of the Humboldt Fellowship and the National Science Foundation CAREER Award. He is the area director for cyber security of the NY State Center for Advanced Telecommunications Technologies at NYU-Poly; Hardware security lead of the Center for research in interdisciplinary studies in security and privacy -CRISSP (http://crissp.poly.edu/), co-founder of the Trust-Hub (http://trust-hub.org/) and organizes the annual red team blue team event at NYU, the Embedded Systems Challenge (http://www.poly.edu/csaw2014/csaw-embedded).

He cofounded the IEEE/ACM Symposium on Nanoscale Architectures (NANOARCH). He is the Program Chair (2012) and General Chair (2013) of IEEE Symposium on Hardware Oriented Security and Trust (HOST). He is the Program Co-Chair (2012) and General Co-Chair (2013) of IEEE Symposium on Defect and Fault Tolerant Nano VLSI Systems. He is the General Chair of the 2009 and 2013 NANOARCH. He is the general co-chair of ICCD 2015, RFIDSEC 2015 and WISEC 2015. He serves on several program committees.

He was the Associate Editor of IEEE Transactions on Information Forensics and Security (2010-2014), IEEE Transactions on CAD (2014-present), ACM Journal of Emerging Computing Technologies (2007-present), ACM Transactions on Design Automation of Electronic Systems (2014-present), IEEE Access (2015-present), IEEE Transactions on Emerging Technologies in Computing (2015-present) and IEEE Design and Test (2015-present). He is an IEEE Computer Society Distinguished Visitor (2013-present). He is on the Executive Committee of IEEE/ACM Design Automation Conference leading the Security@DAC initiative (2014-.)
He has organized/delivered invited tutorials on Hardware Security and Trust (VLSI Test Symposium 2012, 2014, International Conference on Computer Design 2012, IEEE North Atlantic Test Workshop 2013, Design Automation and Test in Europe 2013, IEEE International Test Conference 2014, IEEE/ACM Design Automation Conference 2014, and IEEE LATW 2014).

SISTER CONFERENCE EXCHANGE PAPERS

ISTFA 2014 Outstanding paper

Jörg Jatzkowski, Michél Simon-Najasek (michel.simon-najasek@iwmh.fraunhofer.de) **and Frank Altmann**, Center for Applied Microstructure Diagnostics (CAM), Fraunhofer Institute for Mechanics of Materials, Halle, (Germany) - *Localization of Weak Points in Thin Dielectric Layers By Electron Beam Absorbed Current (EBAC) Imaging*

A novel approach for the localization of weak points in thin transistor and capacitor oxides before electrical breakdown will be presented in this paper. The proposed approach utilizes Electron Beam Absorbed Current (EBAC) imaging based on Scanning Electron Microscopy (SEM). This technique uses the generation of additional charge carriers within the semiconductor substrate level by scanning with a focused electron beam. Over a thin transistor or capacitor oxide layer inside the interaction volume of the electron beam an increased tunnel current is visualized by EBAC and areas with different current intensities indicating weak points become visible. These soft defect areas are investigated in comparison to references which were analyzed by using cross sectioning in a dual beam FIB/SEM system followed by a high resolution Transmission Electron Microscopy (TEM) investigation. The feasibility of this new technique is demonstrated on a defective transistor gate oxide test structure.

Michél Simon-Najasek received his diploma in electrical engineering at the University of Applied Science in Koethen / Germany in 2002. For more than 12 years he has been working in the research group „Diagnostic of semiconductor technologies" at Fraunhofer IWM / CAM in Halle, Germany. Michél´s research field is failure analysis on Si and III/V based electronic devices mainly for automotive applications. He is expert in focused ion beam preparation, electron microscopy analysis and nanoprobing for IC level diagnostics. Michél is coordinating the failure analysis team within his research group.

IPFA 2015 Best paper

Vita Pi-Ho Hu (vitabee@gmail.com), **Pin Su, and Ching-Te Chuang,** Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan - *UTB GeOI 6T SRAM Cell and Sense Amplifier considering BTI Reliability*

The impacts of NBTI and PBTI on the stability of UTB GeOI 6T SRAM cell and performance of sense amplifier compared with the SOI counterparts have been investigated. Worst case stress scenarios for read and write operations are analyzed. For UTB GeOI SRAMs, PBTI dominates the degradations in read static noise margin (RSNM), while for UTB SOI SRAMs, NBTI dominates the degradations in RSNM. Write static noise margin (WSNM) only slightly degrades due to NBTI and PBTI. Current latch sense amplifier (CLSA) and voltage latch sense amplifier (VLSA) are analyzed considering NBTI/PBTI for GeOI and SOI devices. GeOI CLSA and VLSA show smaller word-line to SAE buffer delay and sense amplifier sensing delay than the SOI counterparts. As aging time increases, GeOI CLSA and VLSA show larger degradations of sense amplifier sensing delay than the SOI counterparts.

Vita Pi-Ho Hu received the B. S. degree in department of Materials Science and Engineering and the Ph. D. degree in department of Electronics Engineering & Institute of Electronics from National Chiao Tung University, Hsinchu, Taiwan in 2004 and 2011, respectively. Her research interests include Silicon and IIIV-based nanoelectronics, ultra-low voltage/power SRAM and logic circuits using emerging devices, and device circuit interaction and co-optimization. From 2011 to 2015, she was an Assistant Research Fellow with National Chiao Tung University. She joins National Central University,

Taoyuan, Taiwan as an Assistant Professor in Aug. 2015.

IRPS 2015 Best paper

Ghadeer Antanius (ghadeer.antanius@intel.com), **Rutvi Trivedi and Robert Kwasnick**, Intel Corporation (USA) - *Platform Qualification Methodology: Face Recognition*

Platforms may be developed with a range of new features. We describe a methodology to qualify a platform for operational stability and functional reliability. This includes determining feature-specific goals and use conditions to achieve the desired user experience quality and reliability. We present detailed results for a client PC face recognition feature.

Ghadeer Antanius is an Engineering Manager at Intel Corporation. He is responsible for managing Intel Client Platforms Quality & Reliability including Notebooks, Tablets, Smart Phones and High End Desk Tops. He also manages the Platforms and New Technologies Quality & Reliability Goals and Use Conditions across all Intel market segments. Mr. Antanius holds an Electrical Engineering bachelor's degree. He has two issued US patents.

INVITED PAPERS

- **Christopher Bailey (c.bailey@gre.ac.uk), University of Greenwich -** *Modelling the impact of refinishing processes on COTS components for use in aerospace applications*

This presentation will focus on predictive reliability of commercial off the shelf (COTS) components for high reliability applications in the aerospace and defence sectors. Reliability assessment of newly designed electronic products before their actual manufacture is a critical issue for many organisations. For example, products manufactured by the aerospace industry operate in extreme in-service environments and require very high reliability qualification (e.g. 25-30 years). The limited availability of MiL-Spec components is forcing a number of high reliability markets, to consider the use of COTS electronic components. Many of the COTS components including BGA and QFN packages have not been designed for such high reliability applications. Therefore, characterizing and modelling the behaviour of these components and assessing their reliability and lifetime is a very important task. This presentation details the issues faced by organisations adopting COTS components such as Tin Whiskers and approaches adopted to mitigate these failures. Examples will be provided on the methodologies used to model and predict the reliability of these components and printed circuit boards for aerospace applications and how modelling can help optimise the ruggedisation, reliability and robustness of these components and printed circuit boards.

Chris Bailey is the Professor of Computational Mechanics and Reliability at the University of Greenwich, London, United Kingdom. He received his PhD in Computational Modelling from Thames Polytechnic in 1988, and an MBA in Technology Management from the Open University in 1996. Before joining Greenwich in 1991, he worked for three years at Carnegie Mellon University (USA) as a research fellow in materials engineering. His research has resulted in over 250 publications. He is currently an Associate Editor for the CPMT Transactions and has been a guest editor on the journal of Soldering and Surface Mount Technology. In 2008 he was the General Chair for the IEEE ESTC conference in London and is a regular attendee and committee member of CPMT conferences such as ECTC and EPTC as well as conferences such as Eurosime (Europe), ICEPT (China), and IMPACT (Taiwan). In 2014 he organised the Therminic Conference in Greenwich, London. His research interests are related computational methods for design of engineering components and systems. Chris is a Senior Member of IEEE, Member of IET and is current Vice-President for conferences for IEEE-CPMT society.

- **Koji ERIGUCHI (eriguchi.koji.8e@kyoto-u.ac.jp), Univ. of Kyoto (Japan)** - *Impacts of plasma process-induced damage on MOSFET parameter variability and reliability*

Plasma process-induced damage (PID) is one of critical issues in designing MOSFETs with higher performance and reliability, because PID is believed to enhance the reliability degradation and variability. In this study, damage creation mechanisms during plasma processing — plasma-induced physical damage (PPD) and charging damage (PCD) — are focused on, and the impacts on MOSFET reliability are discussed. In PPD mechanisms, damaged structures result in threshold voltage (V_{th}) shift and drain current decrease of MOSFETs, which are induced by Si recess (Si loss) in the source/drain extension region and the latent defects beneath the damaged region, respectively. The PPD also enhances the MOSFET parameter variability in LSIs due to plasma fluctuation. Model predictions of parameter variability in scaled FinFETs are presented on the basis of the PPD range theory and molecular dynamics simulations, where both stochastic straggling and sputtering play key roles. As for PCD, MOSFETs with high-k dielectrics are shown to suffer from "V_{th}-instability" due to characteristic charge trapping. As a consequence, conflicting results among reliability data such as time-dependent dielectric breakdown (TDDB) lifetime are found under a certain amount of PCD, leading to erroneous conclusions in reliability assignments. Since these mechanisms are unscalable and intrinsic natures of plasma processing, the present PID models should be intensively implemented to design future LSIs with higher performance and reliability.

Koji Eriguchi received the B.S. and M.S. degrees in engineering physics and mechanics from Kyoto University, Japan, in 1989 and 1991, respectively, and the Ph.D. degree in engineering physics from Kyoto University in 2004. He has been an associate professor of Kyoto University since 2005, working on plasma–solid surface interaction, thin dielectric reliability degradation by plasma processing, optical characterization techniques of Si surfaces, and modeling of plasma-induced damage and defect creation in crystalline Si. Prior to joining Kyoto University, he had been a senior engineer at Panasonic from 1991, responsible for the research of plasma etch processes, thin gate dielectric wear-out phenomena including plasma-induced damage (PID), CMOS process integration, and reliability of CMOS devices. He has published more than 80 journal papers and 130 conference papers. He received the Best Paper Award from the 32nd Dry Process Symposium in 2009, the APEX/JJAP Paper Award and the Plasma-Electronics Award from the Japan Society of Applied Physics (JSAP) in 2010.

- **Ludwig BALK (balk@uni-wuppertal.de), University of Wuppertal, Germany -** *EOBT: from past to future*

It is now fifty years ago that both electron beams and laser sources became commercially available to enable inspection techniques for all kinds of applications, but in special for the characterization and the testing of electronics devices. This happened more or less simultaneously with the beginning of integration of electronic components. While at the early times a simple imaging was done only, in the mid 60ies first work was carried out using all kinds of interaction products due to the impact of optical and electron beams to determine device features and their malfunctioning. Those interaction products could well be particles or photons as well as properties like electrical current and voltage. Although these kinds of testing techniques became more and more important, it took more than twenty year that a special conference on this topic was born: the 1st European Conference on Electron and Optical Beam Testing of Electronic devices (EOBT), which was organized in the year 1987 in Grenoble by Bernard Courtois and Eckhard Wolfgang. From then on this conference continued till 1995 as an independent meeting that had attracted several hundreds of scientists and engineers. However, as quite often in research, if a new field becomes mature, the size of a conference reduces, which gave rise to the decision of merging the EOBT with ESREF due to their strong overlap in the field of failure analysis. The EOBT remained an important topic, sometimes as a special session or in other years merged with failure analysis in general. Over the years it had turned out that simple systems cannot always fulfill the tasks needed, due to the reduced sizes of structures and the demand on extreme spatial resolution as well as due to the more and more complicated vertical structure of devices, making it necessary to either prepare devices destructively or to go for sources with high vertical penetration such as for instance ion beams. And last not least so-called hybrid systems came into being enabling the simultaneous measurement of various device properties. The presentation will give a review of some of the important advantages presented in all of the EOBT conferences, without being complete, and it will try to give a view into what may be the needs for future developments.

Professor Dr. Dr.h.c. **Ludwig Josef Balk** studied semiconductor physics at the RWTH Aachen and received his doctoral degree from the faculty of electrical engineering of the same university. After that he joined the department of materials for electrical engineering at the University of Duisburg. In 1991 he became full professor for electronics at the University of Wuppertal, where he was for many years dean of the faculty as well as executive director of the Institute of Polymer Technology. He got several awards, such as various visiting professorships and best papers at conferences. Further he was member of various scientific boards, the most prominent being member of the editorial board of Journal of Physics D for nearly twenty years. His scientific output consists of about 270 publications, out of these 55 invited or keynote papers, over 120 seminars in industry and academic, and 7 international patents.

- **Isik KIZILYALLI (**i.kizilyalli@Avogy.com, kizilyalli@ieee.org**), AVOGY – USA** - *Reliability Studies of Vertical GaN Devices Based on Bulk GaN Substrates*

There is a great interest in wide-bandgap semiconductor devices and most recently in vertical GaN structures for power electronics applications. In this paper, vertical p-n diodes and field-effect transistors fabricated on pseudo-bulk low defect density (10^4–10^6 cm^{-2}) GaN substrates are discussed. Homo-epitaxial low-pressure metal organic chemical vapor deposition growth of GaN on its native substrate and being able to control and balance the n-type Si doping with background C impurity has allowed the realization of vertical device architectures with drift layer thicknesses of 6 to 40 µm and net carrier electron concentrations of 4×10^{15} to 2.5×10^{16} cm^{-3}. This parameter range is suitable for applications requiring breakdown voltages (BVs) of 600 V–4 kV (and higher) with a proper edge termination strategy. Measured p-n diodes demonstrate near power device figure of merit, that is, differential specific on-resistance (R_{sp}) of 2 mΩ-cm2 for a BV of 2.6 kV and 2.95 mΩ-cm2 for a 3.7-kV device, respectively. While, vertical transistors with BV=1500V and R_{sp} of 2.2 mΩ-cm^2 have been fabricated. The improvement in the substrate quality over the last few years has resulted in the fabrication of diodes with areas as large as 16 mm^2, with BVs exceeding 700 V and pulsed (100 µs) currents of 400 A. The structures fabricated are utilized to study in detail the temperature dependence of I–V characteristics, impact ionization based avalanche characteristics and ruggedness, reliability under high-temperature reverse bias, high-temperature operating life, temperature cycling, and temperature-humidity-bias test.

Isik C. Kizilyalli received the B.S., M.S. and Ph.D. (1982, 1984, and 1988) degrees from the University of Illinois in Urbana. His career since spans fundamental research in semiconductors to technology development, commercialization of innovation, and entrepreneurship. Currently, he is the Founder of Avogy Inc. (San Jose, CA) a venture backed start-up concerned with GaN power electronics and power systems. Previously he was with Bell Laboratories, followed by Nitronex Corporation, and solar PV startup Alta Devices where his group holds the world record for single junction solar cell conversion efficiency. Dr. Kizilyalli was elected a Fellow of the IEEE in 2007, received the Bell Laboratories' Distinguished Member of Technical Staff award, and received the Best Paper Award at ISPSD-2013. He has authored or coauthored 100 papers and holds 82 U.S. patents.

- **David GACHET (**david.gachet@attolight.com**), Attolight AG – Switzerland** - *Failure analysis of photonic devices by high-resolution cathodoluminescence*

Quantitative cathodoluminescence (CL) microscopy is a new optical spectroscopy technique that measures optical characteristics over large fields of view with unprecedented spatial resolution without the need for tedious alignment. It is based on the careful intrication of an optical microscope and a custom designed scanning electron microscope (SEM). Thanks to the sensitivity of CL to material composition, as well as to the presence of defect, it is well suited for device characterization at sub micron scale. Here we present a selection of failure analyses and ageing effect studies performed with quantitative CL on optoelectronic devices.

David Gachet got a PhD in physics from the University of Aix-Marseille, France (2007) working on novel non-invasive contrasts in optical microscopy for biology. He then worked two years and a half (2008-2010) as a postdoctoral researcher at Weizmann Institute of Science (Rehovot, Israel) and Fresnel Institute (Marseille, France) in the field of optical spectroscopy and microscopy of nanoparticles. In 2010, he was appointed Assistant professor at the University of Aix-Marseille (France). Since 2013, he has been leading the Analytical laboratory of the Swiss company Attolight. The laboratory specializes in defect metrology and failure analysis in semiconductor devices using quantitative cathodoluminescence microspectrometry.

- **Alain BENSOUSSAN et al, IRT Saint-Exupéry (F) - Permanent address: Thales Alenia Space (F),** *A unified multiple stress reliability model for microelectronic devices – Application to 1.55 µm DFB laser diode module for space validation*

The establishment of European suppliers for DFB Laser Modules at 1.55 µm is considered to be essential in the context of future European space programs, where availability, cost and schedule are of primary concerns. Also, in order to minimize the risk, associated with such a development, the supplier will be requested to use components, which have already been evaluated and/or validated and/or qualified for space applications. The Arrhenius model is an empirical equation able to model temperature acceleration failure modes and failure mechanisms. The Eyring model is a general representation of Arrhenius equation, which take into account additional stresses than temperature. The present paper suggests to take advantage of these existing theories and derives a unified multiple stress reliability model for electronic devices in order to quantify and predict their reliability figures when operating under multiple stress in harsh environment as for Aerospace, Space, Nuclear, Submarine, Transport or Ground. Application to DFB laser diode module technologies is analyzed and discussed based on evaluation test program under implementation.

Alain Bensoussan is engineer in Applied Physics from Institut National des Sciences Appliquées (INSA), Lyon (France), in 1979 and Doctor Engineer from INSA Toulouse (France) in 1984. He has been 7 years with the Centre National de la Recherche Scientifique (CNRS) at L.A.A.S. (Laboratoire d'Analyse et d'Architecture des Systèmes) to complete his ''Thèse d'Etat'' working on design and development of laser diode devices. Since 1987, he joined Thales Alenia Space, as now Senior Engineer with 32 years expertise in EEE parts including Microwaves, MEMS and Optoelectronic devices. He represented Thales Alenia Space at EUROSPACE organization, nominated by the "Eurospace" organization to support the Space Components User interests at ESA - PSWG (European Space Agency - Parts Policy and Standards Working Group) since more than 15 years. He is now, full time seconded at Institut de Recherche Saint Exupéry, (Aeronautic, Space and Embedded Systems - AESE), Toulouse (France).

- **Stéphane MOREAU (stephane-nico.moreau@cea.fr), CEA-LETI (F),** *Electromigration, still a reality for 3D ICs ?*

3-D integration is booming, however, like any new integration/product, before being put on the market, it is necessary to check its reliability. This presentation focuses on the electromigration phenomenon, a degradation of metal levels, which could lead to open circuits or possibly a short circuit, in the interconnections of future products (3DIC) integrating the 3-D approach. First, we address the problem in the case of an intra-chip interconnect, high density TSV-last (Ø3 µm × 15 µm) and then, in a second time, for inter-chip interconnect, Cu/SiO_2 hybrid bonding. For these two case studies, the traditional main theme of a reliability study will be followed: test structures, tests, statistical analysis and failure analysis (fault location, morphological analysis, in situ SEM). The presentation will conclude on the problem of modeling the electromigration phenomenon.

Stéphane Moreau received his PhD in Electronics from François-Rabelais University (Tours, France) in 2005 on the environmental reliability of TRIAC (semiconductor switch), work done with STMicroelectronics (Tours, France). In 2006, he joined CEA-LETI (Grenoble, France) first as a postdoctoral fellow and then, in 2008, as a research engineer. His research areas include multiphysics simulations and reliability issues, especially electromigration and environment-induced damage (CTE mismatch, humidity,…) for 3-D integration. He has authored or co-authored of more than 30 papers on those topics and served on the IRPS conference as reviewer.

- **Takashi SETOYA (takashi.setoya@toshiba.co.jp), Toshiba Corp (Japan),** *Destruction Failure Analysis and International Reliability Test Standard for Power Devices*

As for the demand for semiconductor power device, it is predicted these are growing drastically in future for EV/HEV and Natural energy connections. The power devices are affected by the stress unlike the normal semiconductor device including a big electric current, the sudden temperature change, and it is an important problem how to guarantee the reliability. Therefore For power device, special evaluation methods and confirmation method are necessary. On the other hand, the trend such as publishing power semiconductor qualification guideline for vehicle is coming out of Japan. In this presentation are shown reliability test method, destruction measures, screening method, and failure analysis techniques for semiconductor power devices. Furthermore, this presentation is introducing an international standard trend of power devices.

Takashi Setoya is Chief Quality Executive of TOSHIBA Corporation Semiconductor & Storage Products Company, responsible for Reliability and Quality of discrete, Logic, analog, memory, SSD and HDD products. He joined TOSHIBA in1983. He is working for the quality and reliability of semiconductor more than 30years. He holds a bachelor's degree from HOSEI University, and He is a chairman of JEITA semiconductor technology reliability Committee, and a director of RCJ(Reliability center of Japan). He is married and has three children.

- **Guillaume AUDOIT (guillaume.audoit@cea.fr), CEA-LETI (France) -** *"Plasma FIB development for 3D IC structures investigations and X-ray tomography sample preparation"*

To continue the increases in speed and density of microelectronic systems described by Moore (More Moore), 3D integration seems to be the next revolution in the IC industry. One major challenge of these architectures, which basically consist in stacking vertically different components, is the manufacturing and the associated reliability and monitoring of the interconnections in between the components. The ability to physically characterize the interconnections such as through silicon vias (TSV) used in 3D integration is essential for developing robust manufacturing processes and fabricating reliable products. Focused ion beam (FIB) systems have long provided both physical analysis (FIB/SEM) and sample preparation such as TEM lamellae, but conventional FIB cannot remove material fast enough to analyze the relatively large 3DIC structures. The high milling rate of the Plasma FIB technology has been developed to address these needs. We present here some developments for high rate ion induced metal deposition using a co-axial needle as a gas injection system and also beam parameters optimization for large milling of curtain free cross sections (example of a TSV). Furthermore, we present how the plasma FIB can be used as a very efficient way of preparing samples for X-ray tomography to investigate large 3D structures.

Guillaume Audoit obtained his engineer degree (M.S.) from the national school of chemistry in Montpellier in 2002 and a PhD in nanoscience in 2005 from the University College Cork. He spent 4 years in the industry working in physico-chemical characterization by FIB/SEM and TEM of a wide variety of inorganic materials. In 2010, he joined the nano-characterization platform of CEATech/Leti on Minatec campus Grenoble (France) to work on the sample preparation by focused ion beam for Transmission Electron Microscopy, Atom Probe Tomography, Secondary Ion Mass Spectrometry and Atomic Force Microscopy. He is now in charge of the sample preparation group, including more general preparation approaches such as mechanical polishing, accurate cleaving and dicing, chemical attack and broad beam ion milling. Its main fields of interest and experience include silicon-based microelectronics, 3DIC, sensitive materials preparation (GaAs, InP, GaN, etc…) and materials for new energies.